The invention claimed is:

1. A circuit arrangement for a reception part of an SDH (=Synchronous Digital Hierarchy) transmission system for transmitting plesiochronous signals, comprising

- a plurality of input channels allocated to the plesiochronous signals, the intput channels being connected to a clock synchronizer for adapting the received plesiochronous signals to a common processing clock, and

- a reception multiplexer following the clock synchronizer, with reception processing means being connected at its output for transforming a plesiochronous signal into a synchronous signal for an SDH transmission channel.

2. The circuit arrangement of Claim 1 wherein the clock synchronizer contains a plurality of buffer memories corresponding to the plurality of input channels for writing in the signals with their plesiochronous signal clock, and for reading out the signals with a synchronous processing clock.

3. The circuit arrangement of Claim 1 further comprising a demultiplexer following the reception-processing means .

4. A circuit arrangement for a transmission part of an SDH transmission system for transmitting plesiochronous signals, comprising

a transmission multiplexer, at the output of which a transmission processing means for transforming a transmitted synchronous signal into a plesiochronous signal is connected, and

a desynchronizer following the transmission processing means for recovery of the plesiochronous signal clocks of the plesiochronous signals and to issue the plesiochronous signals to a plurality of output channels.

5. The circuit arrangement of Claim 4, wherein the transmission processing means is connected to a transmission demultiplexer contained in the desynchronizer.